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5	BRS	L18	0	(non-interchangeable same cable) and emulation	USPAT	2005/10/25 14:54
6	BRS	L19	9	(non-interchangeable same cable)	USPAT; IBM_TDB	2005/10/25 14:55
7	BRS	L20	1	non-interchangeable near cable	USPAT; IBM_TDB	2005/10/25 14:55
8	BRS	L21	0	non-interchangeable near conductor	USPAT; IBM_TDB	2005/10/25 14:55
9	BRS	L22	6	non-interchangeable same conductor	USPAT; IBM_TDB	2005/10/25 14:56
10	BRS	L23	1	"5644515".pn.	USPAT; IBM_TDB	2005/10/25 14:56
11	BRS	L24	1	"5644515".pn. and (conductor or cable)	USPAT; IBM_TDB	2005/10/25 15:00
12	BRS	L25	1	"5963735".pn. and (conductor or cable)	USPAT; IBM_TDB	2005/10/25 15:00
13	BRS	L26	1	"5960191".pn. and (conductor or cable)	USPAT; IBM_TDB	2005/10/25 15:37
14	BRS	L27	1	"5960191".pn. and (conductor or cable) and test	USPAT; IBM_TDB	2005/10/25 15:00
15	BRS	L28	1	"5644515".pn. and (conductor or cable) and test	USPAT; IBM_TDB	2005/10/25 15:15
16	BRS	L29	1	"5963735".pn. and (conductor or cable) and test	USPAT; IBM_TDB	2005/10/25 15:00
17	BRS	L30	28	(cable adj length) and (logic adj design)	USPAT; IBM_TDB	2005/10/25 15:16
18	BRS	L31	0	(cable adj length) and (logic adj design) and (conductors same interchange$)	USPAT; IBM_TDB	2005/10/25 15:16
19	BRS	L32	0	(cable adj length) and (logic adj design) and (non-interchangeable)	USPAT; IBM_TDB	2005/10/25 15:16
20	BRS	L33	0	(cable adj length) and (non-interchangeable)	USPAT; IBM_TDB	2005/10/25 15:17
21	BRS	L34	251	(non-interchangeable)	USPAT; IBM_TDB	2005/10/25 15:17
22	BRS	L35	43	(non-interchangeable) and cable	USPAT; IBM_TDB	2005/10/25 15:17
23	BRS	L36	1	(non-interchangeable) and cable and logic	USPAT; IBM_TDB	2005/10/25 15:18
24	BRS	L37	1342	logic same emulation	USPAT; IBM_TDB	2005/10/25 15:19
25	BRS	L38	48	(logic same emulation) and (cable same length)	USPAT; IBM_TDB	2005/10/25 15:19
26	BRS	L39	33	(logic same emulation) and (cable same length) and (circuit adj board)	USPAT; IBM_TDB	2005/10/25 15:20
27	BRS	L40	1	"6618698".pn.	USPAT; IBM_TDB	2005/10/25 15:43

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28	BRS	L41	0	"6618698".pn. and interchange	USPAT; IBM_TDB	2005/10/25 15:43
29	BRS	L42	368	703/23.ccls.	USPAT	2005/10/25 15:44

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J Kumar, N Strader, J Freeman, M Miller, AD ... - Computer Design: VLSI in Computers and Processors, 1995. ..., 1995 - ieeexplore.ieee.org
... Abstract: Large-scale **hardware logic emulation** using software configurable hardware provides a new means to significantly improve verification of complex ...
Cited by 13 - Web Search - portal.acm.org - portal.acm.org - csa.com

Commercial Design Verification: Methodology and Tools
C Pixley, NR Strader, WC Bruce, J Park, M Kaufmann ... - The 1996 IEEE International Test Conference, 1996 - doi.ieeecomputersociety.org
... Large-scale **hardware logic emulation** using software con- figurable hardware provides a relatively new means to sig- nificantly improve pre-tape-out ...
Cited by 16 - Web Search - ieeexplore.ieee.org - portal.acm.org - csa.com - all 6 versions »

Prototyping the M 68060 for concurrent verification
J Kumar - IEEE Design & Test of Computers, 1997 - ieeexplore.ieee.org
... Large-scale **hardware logic emulation** can create a func- tional design prototype that executes almost six orders of magnitude faster than classical simulation. ...
Cited by 10 - Web Search - portal.acm.org - portal.acm.org - csa.com - all 5 versions »

Using Dynamically Reconfigurable Hardware in Real-Time Communications Systems
A Carter - University of York Department of Computer Science, Real Time ..., 2001 - cmsa.wmin.ac.uk
... types of FPGA available, and the uses to which they can be put, [Hauck98] gives the following types of application: • **Hardware logic emulation** (faster than ...
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Emulation Verification of the Motorola 68060
M Inc - ieeexplore.ieee.org
... Abstract Large-scale **hardware logic emulation** using software configurable hardware provides a new means to significantly improve verification of complex ...
Web Search

Logic and Functional Verification in a Commercial Semiconductor Environment
M Inc, J Kumar, C Pixley - doi.ieeecs.org
... Large-scale **hardware logic emulation** can create a functional design prototype that executes almost six orders- of-magnitude faster than classical simulation. ...
Web Search - ieeexplore.ieee.org - doi.ieeecomputersociety.org

In-System Design Verification of Processors
D Hierarchy - vswww.kaist.ac.kr
... 10 5 10 4 10 3 10 2 10 1 1 Actual **Hardware Logic Emulation** Software Simulation Verification Gap Page 5. Concurrent Verification Early to Market!! Design Code ...
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Using Dynamically Reconfigurable Hardware for Real-Time Lossless JPEG Encoding
A Carter, MS Thesis - cmsa.wmin.ac.uk
Page 1. Using Dynamically Reconfigurable Hardware for Real-Time Lossless JPEG

Encoding Alison Carter March 2004 MSc Thesis Page 2. Abstract ...
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New Methods for Tolerance Analysis in Solid Modeling
JU Turner - ... Integrated Manufacturing, 1988., International Conference on, 1988 - ieeexplore.ieee.org
Page 1 0-8186-0888-9/88/0000/0306/$O1.0O iCi 1988 IEEE New Methods for Tolerance Analysis in Solid Modeling Joshua U. Turner IBM Corporation Dept. C13/I3ldg. ...
Web Search - ieeexplore.ieee.org

Tolerances in computer-aided geometric design
JU Turner, MJ Wozny - The Visual Computer, 1987 - springerlink.com
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S Modeling - ieeexplore.ieee.org
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Code verification by hardware acceleration
H Kohler, J Kayser, H Pape, H Ruffner - ASIC/SOC Conference, 2001. Proceedings. 14th Annual IEEE ..., 2001 - ieeexplore.ieee.org
... ET3 is not based on FPGA's but on a huge number of very small **emulation** processors. **...**
as a processor instruction in one of these **emulation**-processors. **...**
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[PS] Recommended Resources for Teaching Discrete Mathematics
DS Franzblau, JC Kowalczyk - dimacs.rutgers.edu
... imaging. Excursions in Modern Mathematics (9{College) **Peter Tannenbaum** and Robert Arnold; Prentice-Hall, 2nd Ed., 1995; $57. This ...
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standalone or in-**circuit emulation** modes in its smallest. configuration (Fig. 1). ... FPGAs on multiple **boards interconnected** by backplanes. ...
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Logic simulation. is a critical. step in the **design** of a **logic circuit**. ...
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EP patents matching keyword '**logic**'
EP259662, Method for generating a candidate list of faulty **circuit** elements and Method for isolating faults in a ... EP598149, **Hardware logic** simulator. ...
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gate **boards**. Results, including in-**circuit Emulation** of a ... **Logic design**, described by a netlist, across an **interconnected**. **Logic**. Simulation. Accelerated ...

www.eecs.umich.edu/~valeria/ teaching/eecs578_W05/papers/bab97.pdf - Supplemental Result - Similar pages

Routing methods for use in a **logic emulation** system - US Patent ...
... wherein such a reconfigurable hardware **emulator** is used ... a gate array chip or printed **circuit board** into the ... distinct from the **logic** chips being **interconnected**. ...
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Hardware logic emulation system capable of probing internal nodes ...
a microprocessor in-**circuit** emulator includes a **cable** which can be plugged into
a system ... and signal routing between fixed **printed circuit board** traces. ...
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Hardware logic emulation system - US Patent 5963735
an **Hardware logic emulation** system comprising: A **printed circuit board** having an
... A microprocessor in-**circuit** emulator includes A **cable** which can be ...
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EP985175 Quickturn european software patent - Distributed logic ...
in a presently preferred embodiment, each **printed circuit board** contains fifty-four
... The Control **board** 600 also generates The trace and functional **test** ...
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Proportional to the number of events (**circuit** size* no. of cycles*Event density)
... **cable**. PSG. (pin Signal Generator). daughter **board**. chip model;ISS ...
www.ce.rit.edu/~631/Verification.Tutorial.ppt - Supplemental Result - Similar pages

United States Patent Application: 0050114113
the method of claim 2, further comprising: instructing a **cable** controller to ...
a testbench is a Series of **test** vectors (ie, stimulus) that are used to ...
appft1.uspto.gov/.../ 20050114113&RS=DN/20050114113 - 65k - Supplemental Result - Cached - Similar pages

Bandwidth Market, Ltd
in A presently preferred embodiment, each **printed circuit board** contains fifty-four
... The Control **board** 600 also generates The trace and functional **test** ...
bandwidthmarket.com/resources/ patents/apps/2002/10/20020161568.html - 256k - Supplemental Result - Cached - Similar pages

Emulation system with time-multiplexed interconnect - United ...
Horstmann, "Marco **Test circuit** Generation," IBM TDM vol. ... A set of fixed
Electrical conductors of said **printed circuit board** Connecting said programmable ...

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Improving generator availability by use of strategic spares
NW HODGES - POWER ENGINEERING JOURNAL, 1989 - ieeexplore.ieee.org
... Although **conductor** faults were the principal ... manufacturer's units, the exciters were not all identical and that at least three **non interchangeable** designs were ...
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